Electronic Version
Stylesheet Version v1.1.1

SEMICONDUCTOR EMBEDDED MEMORY DEVICES HAVING BIST CIRCUIT SITUATED UNDER THE BONDING PADS

Abstract

An embedded memory chip having BIST (built-in self test) circuit under pad is disclosed. The embedded memory chip includes a logic circuit and a memory unit coupled to the logic circuit. The logic circuit and memory unit are fabricated substantially in a center area of the embedded memory chip. A number of bonding pads are situated on a peripheral area adjacent to the center area of the embedded memory chip. The BIST circuit is situated directly under at least one of the bonding pads. The BIST circuit is activated when implementing an IC testing on the embedded memory chip for detecting faults in the memory unit and is deactivated as a disuse part of the embedded memory chip after finishing the IC testing.